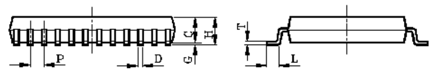
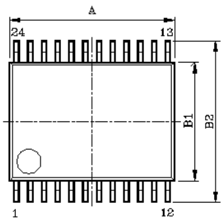
KIA2051FN

BIPOLAR LINEAR INTEGRATED CIRCUIT

AM PULSE NOISE REDUCTION

KIA2051FN is designed for AM stereo pulse noise reduction. The AM stereo pulse noise reduction IC can be easily combined with main tuner RF processor KIA2074F. This IC is very good pulse noise reduction characteristic.





DIM	MILLIMETERS
A	7.8±0.2
B1	5.6±0.2
B2	7.8±0.3
C	1.2±0.2
D	0.22±0.1
G	0.1+0.1/−0.05
H	1.6 MAX
L	0.45±0.2
P	0.65
T	0.15+0.1/−0.05

NMFP−24

FUNCTIONS

- IF AGC.
- AF AGC.
- NOISE AGC.
- AM detection.
- Noise amp.
- Operating supply voltage : V_{opr}=8±1V.
- Pulse noise detection.
- Gate.
- Wave compensation.

MAXIMUM RATINGS (Ta=25℃)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	10	V
Power Dissipation (Note)	P_D	550	mW
Operating Temperature	T_{opr}	-40~85	℃
Storage Temperature	T_{stg}	-55~150	℃

Note : Derated above Ta=25℃ in the proportion of 4.4mW/℃.

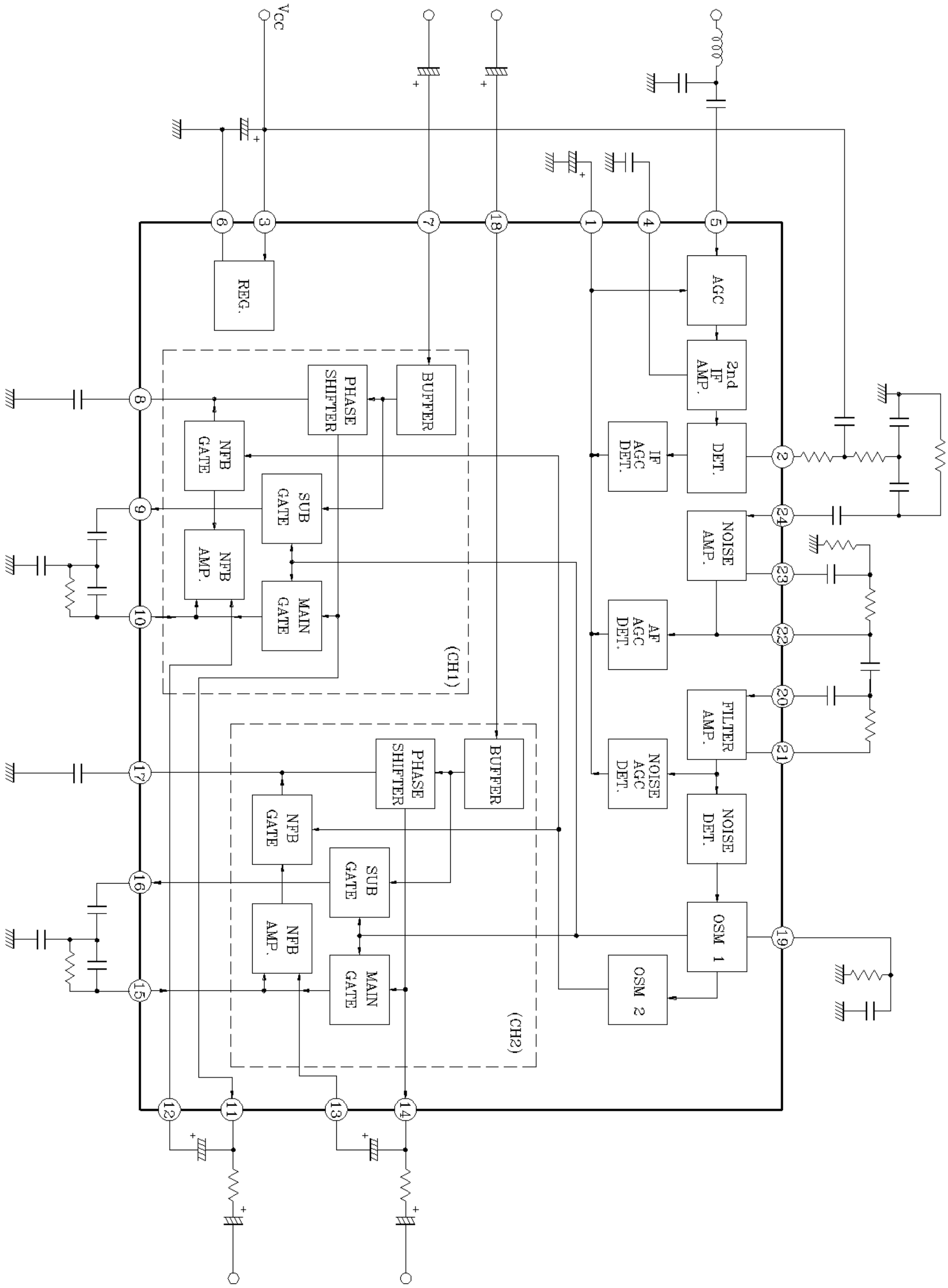
ELECTRICAL CHARACTERISTICS (Unless otherwise specified, V_{CC}=8.5V, Ta=25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current	I_{CC}	V_{IN}=0	25	35	45	mA
DETECTION						
IF Input Impedance	Z_{id}		-	50	-	kΩ
IF Amp. Gain	G_{VD}	f=450kHz, V_{IN}=100μV_{rms}(40dBμV) f_{mod}=1kHz, 100%	51	54	57	dB
IF AGC Level	AGCi	f=450kHz, V_{IN}=178mV_{rms}(105dBμV) f_{mod}=1kHz, 100%	-12	-10	-7	dBV
IF Remaining Noise	vni	V_{IN}=-20dBμV	-	-43	-27.2	dBV
AGC Change Width	AGC_W	f=450kHz, V_{IN}=178mV_{rms}(105dBμV) f_{mod}=1kHz, 100%	-	-25	-14	dBV
Noise Amp. Gain	G_{VN}	f=15kHz, V_{IN}=1mV_{rms}	36	39	42	dB
Noise AGC Level	AGC_N	f=15kHz	-21.2	-18.7	-16.7	dBV
Noise Detection Ratio	P/A	f=15kHz	5.5	7.5	9.5	dB
Filter Feed Back Gain	G_{vf}	f=15kHz	0.4	0.8	1.2	dB
AF AGC Ratio	A'/A	f=15kHz	1.8	3.8	5.8	dB
AGC Current	Ia		24	30	45	μA
AGC Current Ratio	R_{dc}		-10	-9	-8	-
GATE						
Voltage Gain	G_V	f=400Hz, V_{IN}=400mV_{rms}	-2.0	-1.0	0.5	dB
Total Harmonic Distortion	THD_0	f=400Hz, V_{IN}=700mV_{rms}	-	0.1	1.0	%
Total Harmonic Distortion	THD_1	f=400Hz, V_{IN}=400mV_{rms}	-	0.05	0.2	%
Sub Gate Voltage Gain	G_{VS}	f=400Hz, V_{IN}=400mV_{rms}	5	6	7	dB
Compensation Total Harmonic Distortion	THD_2	f=400Hz, V_{IN}=400mV_{rms} T_{SW}=0.3mS, T=9mS	-	2.5	4.0	%
Channel Separation	CS	f=400Hz, V_{IN}=400mV_{rms}	50	80	-	dB
Noise Reduction Output	Nr	T_{SW}=0.3mS, T=9mS Din Noise Peak	-	-62.2	-55.2	dBV
Input Impedance	Zig		-	30	-	kΩ
Output Impedance	Zog		-	500	-	Ω

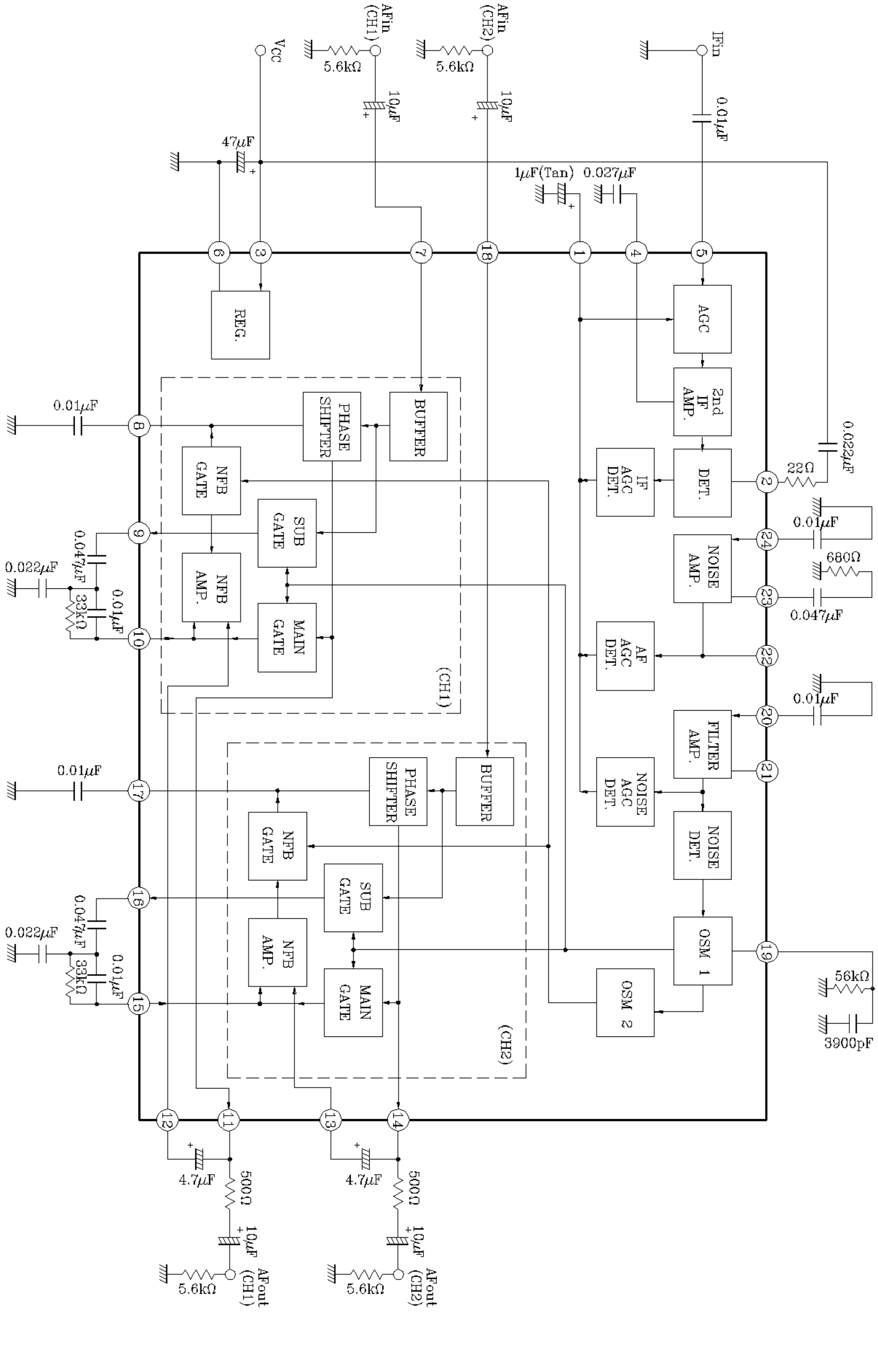
TERMINAL NAME

PIN NO.	SYMBOL	NAME
1	AGC	AGC
2	Det.-out	Detector Output
3	V_{CC}	Supply Voltage
4	IF Bypass	IF Amp. Bypass
5	IF in	IF Input
6	GND	Ground
7	AF in 1	Audio Signal Input 1
8	Phase Shift 1	Phase Shifter 1
9	Sub Gate-out 1	Sub Gate Output 1
10	Main Gate-out 1	Main Gate Output 1
11	AFout 1	Noise Cancel Output 1
12	NFB Amp.-out 1	NFB Amp. Output 1
13	NFB Amp.-out 2	NFB Amp. Output 2
14	AFout 2	Noise Cancel Output 2
15	Main Gate-out 2	Main Gate Output 2
16	Sub Gate-out 2	Sub Gate Output 2
17	Phase Shifter 2	Phase Shifter 2
18	AF in 2	Audio Signal Input 2
19	TPW Trimmer	Trigger Pulse Width Control.
20	Filter Amp.-in	Filter Amp. Input
21	Filter Amp. Feed Back	Filter Amp. Feed Back
22	Noise Amp.-out	Noise Amp. Output
23	Noise Amp. Bypass	Noise Amp. Bypass
24	Noise Amp.-in	Noise Amp. Input

BLOCK DIAGRAM



TEST CIRCUIT



TEST METHOD

1. Circuit (I_{CC}) Fig. 1

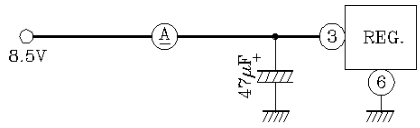


Fig. 1

2. IF impedance (Zid) Fig. 2

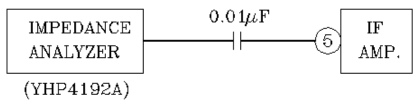


Fig. 2

3. IF Amp. Gain (Gvd) Fig. 3

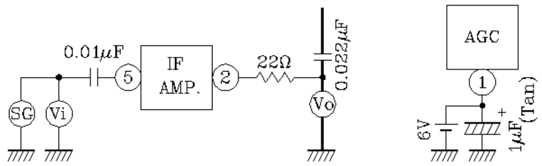


Fig. 3

4. IF AGC Level (AGCi) Fig. 4

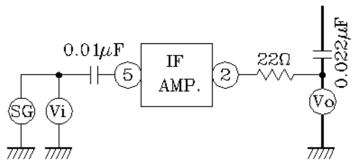


Fig. 4

5. IF Remaining Noise (V_{NI}) Fig. 5

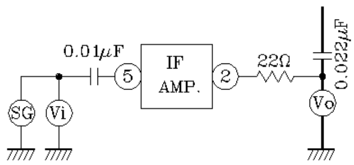


Fig. 5

6. AGC Change Width (AGCw) Fig. 6

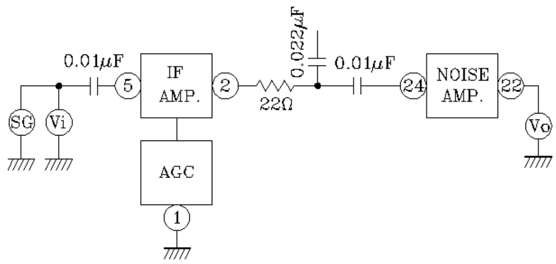


Fig. 6

7. Noise Amp Gain (G_{VN}) Fig. 7

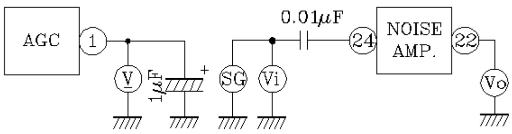


Fig. 7

8. Noise AGC Level (AGC_N) Fig. 8

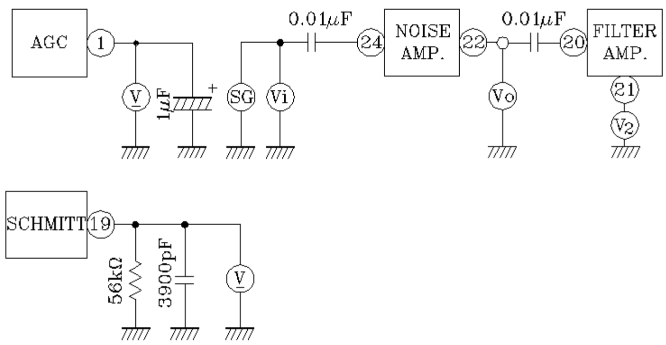


Fig. 8

9. Noise Detection Ratio (P/A)
   $P/A=V_1'dBV-AGC_N(=V_1)$ dBV AGC_N : Noise AGC Level.
   (V_1'dBV : ㉒ Pin Output Voltage at ⑲ pin in 3V)

10. Filter Feed Back Gain (Gvf)
    $Gvf=V_2dBV-V_1dBV$

11. AF AGC Ratio (A'/A)
    $A'/A=Vo'dBV-AGC_N(=V_1)dBV$ AGC : Noise AGC Level.

12. AGC Current (Ia)
    at Switch off : Fig. 9

13. AGC Current Ratio (R_{dc})
    Rdc=Ia'/Ia (at switch on : Fig. 9)

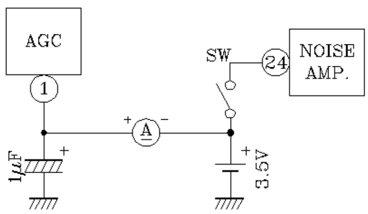


Fig. 9

14. Voltage Gain (G_V) Fig. 10

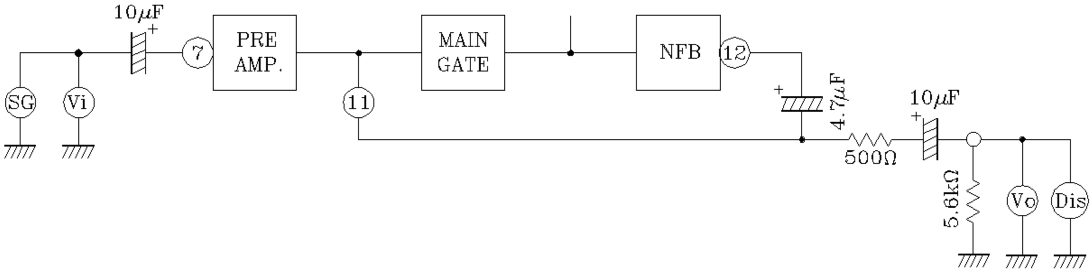


Fig. 10

15. Total Harmonic Distortion (THD_0) Fig. 10

16. Total Harmonic Distortion (THD_1) Fig. 10

17. Sub Gate Voltage Gain (Gvs) Fig. 11

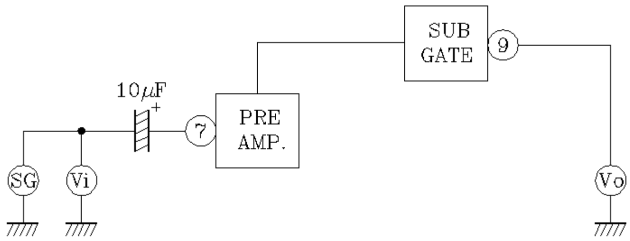


Fig. 11

18. Compensation Total Harmonic Distortion (THD2) Fig. 12

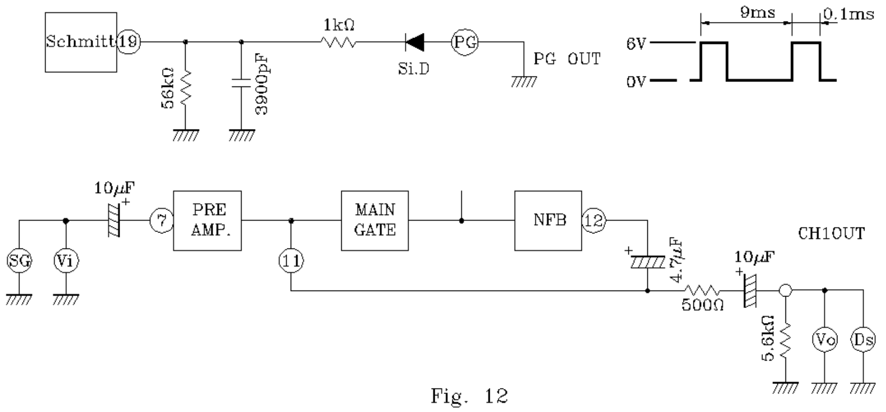


Fig. 12

19. Channel Separation (CS) Fig.13

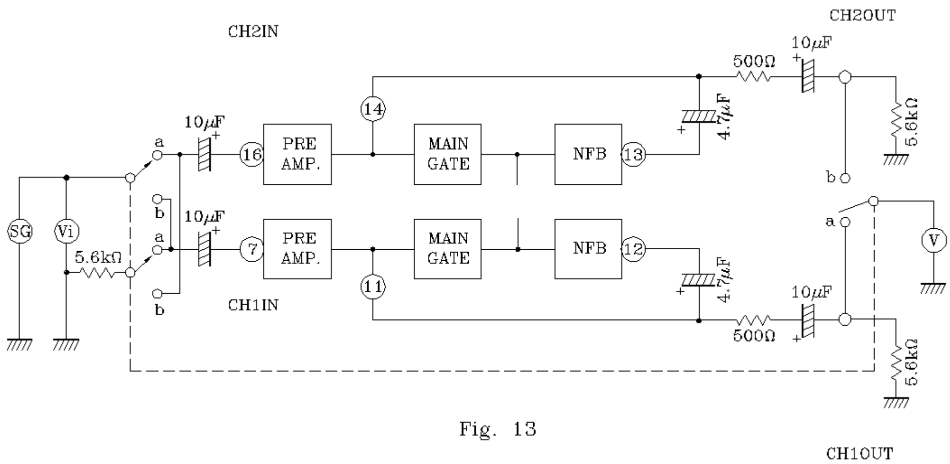


Fig. 13

20. Input Impedance (Zis) Fig. 14

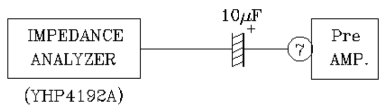


Fig. 14

21. Output Impedance (Zos) Fig. 15

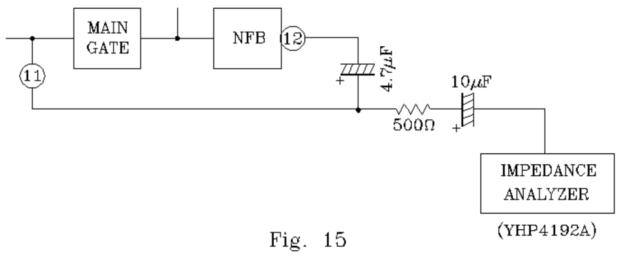


Fig. 15

22. Method of Noise Reduction Output Test. Fig. 16

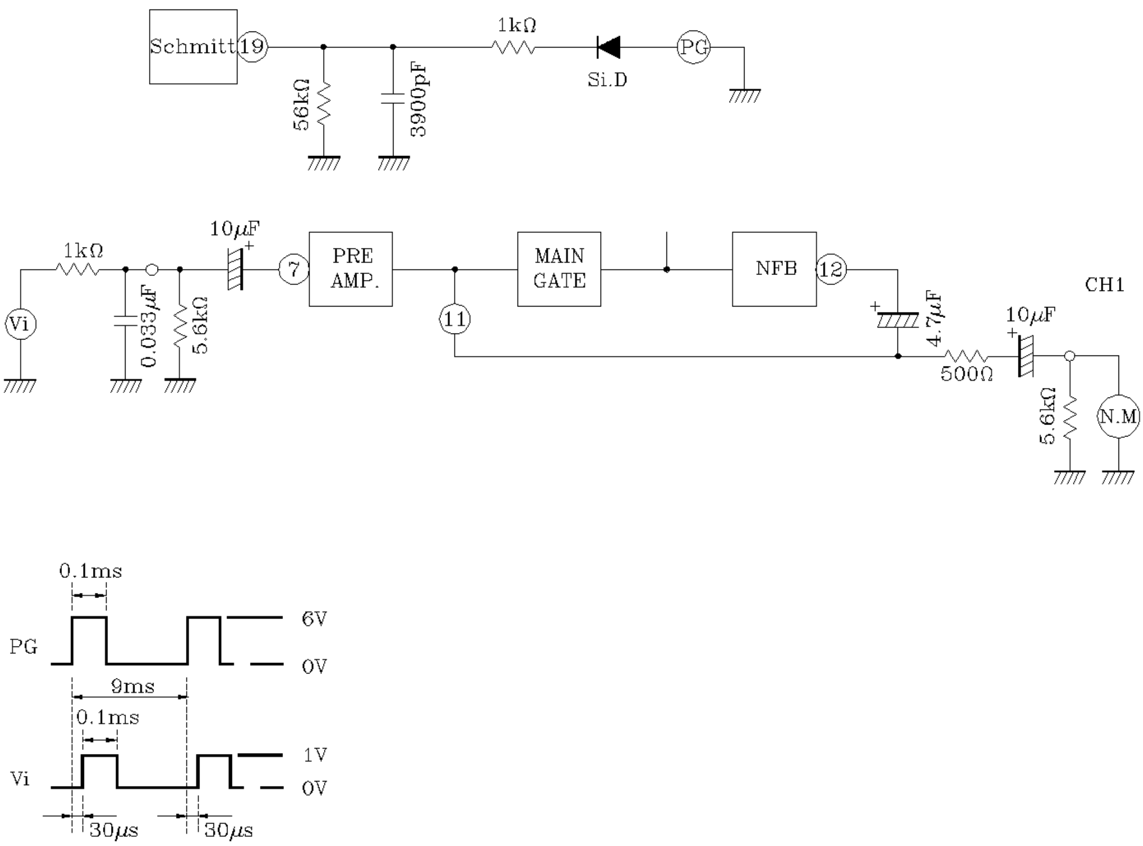
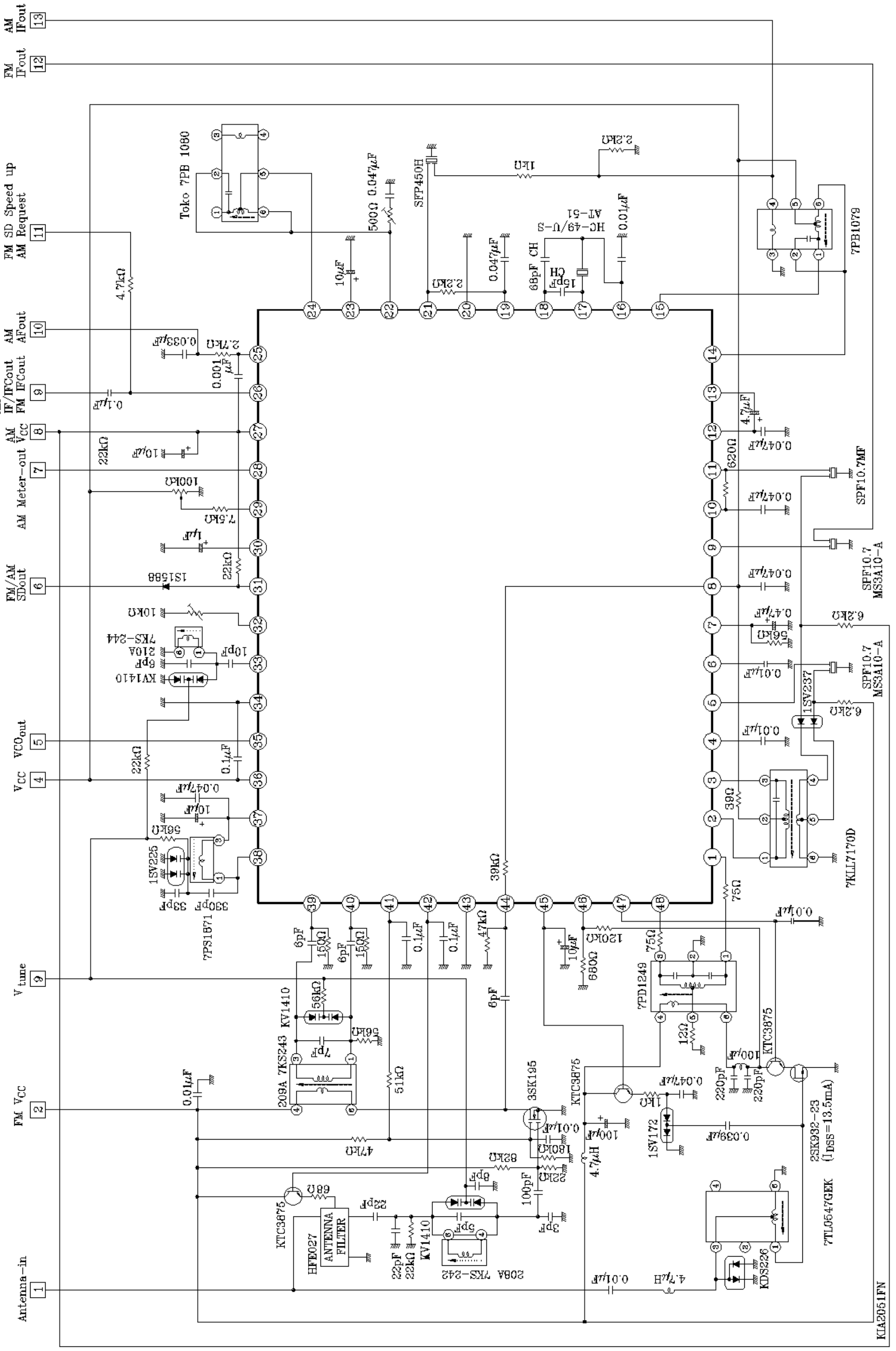


Fig. 16

APPLICATION CIRCUIT



APPLICATION CIRCUIT